REMARKS

The following amendment amends the Specification, the Claims, and the Drawings. More specifically, in the Specification the paragraph beginning on line 10, page 12 is amended to correct a typographical error and likewise the paragraph beginning on line 19, page 15 is amended to correct a typographical error, no new matter is added and no new issues are raised. Claims 1-4, 6-12, 14, 16, 17, 19-22, 25, 27, 29-32, 34-39, 41, 43-45, and 47-49 are amended along with Figure 2 in the drawings, no new matter and no new issues are raised by these amendments. Now in the application are Claims 1-49 of which Claims 1, 21, 22, 28, 29, and 49 are independent. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance.

Amendments to the Specification:

The paragraph beginning on line 10, page 12 of the application is amended to replace the term "portion" on line 12 with the term "pointer" to correct a typographical error and coincide with the remainder of the Specification. The amendment to the paragraph beginning on line 19, page 15 amends the step reference number and the figure identified on line 13, page 16. Specifically, reference identifier (52) is replaced with reference identifier (62), and Figure 3 is replaced with Figure 4 to coincide with the drawing in Figure 4.

Claim Amendments:

Claims 2-4, 6-12, 14, 16, 17, 19-21, 25, 27, 30, 31, 34-39, 41, 43-45, and 47-49 are amended to address antecedent basis issues identified by the Examiner and are not meant to address any art rejection. Further, Claim 22 is amended to recite a portion of the subject matter recited in Claim 26 as originally filed.

Amendment to the Drawings:

Applicant's amend Figure 2 to remove reference identifier (42) and to add the label "Rows" in two places under the numbers "64" shown in the right hand portion of the drawing to improve the understanding of Figure 2 and coincide with the Specification. No new matter is added.

OBJECTION TO SPECIFICATION

The title of the invention stands objected to as non-descriptive. Applicant's respectfully contend that the original title "A Flushable Free Register List" is clearly indicative of and descriptive of the invention to which the claims are directed. Specifically, each independent claim recites either a structure to track register allocation for a microprocessor or alternatively recites a structure for holding information identifying available physical registers for a microprocessor. Clearly, one skilled in the art would readily recognize from the as filed Title of The Invention that the invention to which the claims are directed is a flushable free register list. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the objection to the specification.

OBJECTION TO THE DRAWINGS

A. Objection under 37 C.F.R. §1.84(p)(5):

The drawings stand objected for failing to comply with 37 C.F.R. §1.84(p)(5). Specifically, reference signs "42" and "62" and "64" are objected to for not being mentioned in the detailed description of the Specification. Applicants amend Figure 2 to remove reference sign "42" and amend the Specification to replace the reference sign "52" with the reference sign "62" shown on page 16, line 13. With regard to reference sign "64", Applicants respectfully direct the Examiner's attention to page 16, line 18, of the Specification where step 64 in Figure 4 is referred to and discussed. Accordingly, in view of the amendment to Figure 2 and the Specification, Applicants

respectfully request the Examiner to reconsider and withdraw the objection to the drawings under 37 C.F.R. §1.84(p)(5).

B. Objection under 37 C.F.R. §1.83(a):

The drawings also stand objected to under 37 C.F.R. §1.83(a) for failing to show every feature of the invention specified in the claims. Specifically, the features recited in Claims 18 and 46 concerning the performance of the claimed method in a modulo-8 memory array. Applicants' respectfully direct the Examiner's attention to Figure 1. Figure 1 illustrates a microprocessor suitable for practicing the illustrative embodiment of the invention. Figure 1 includes graphical box symbol labeled "Memory Array 16". Hence, in accordance with 37 C.F.R. §1.83(a) the features recited in Claims 18 and 46 are properly illustrated. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of the drawings under 37 C.F.R. §1.83(a).

CLAIM REJECTIONS

A. Claim Objections under MPEP §608.01(n):

Claims 5-17, 19-20, 34-45, 47, and 48 stand objected to for improper dependent form. MPEP §608.01(n) is cited in support of the objection. Nevertheless, Applicants respectfully choose to defer the renumbering of the Claims until allowable subject matter is identified to avoid further confusion during prosecution. Accordingly, Applicants respectfully request the Examiner to continue the objection under MPEP §608.01(n) until an indication of allowable subject matter.

B. Objection to Claim 22:

Claim 22 stands objected to for a typographical error. Accordingly, Applicants amend Claim 22 to correct the typographical error and request the Examiner to reconsider and withdraw the rejection to Claim 22 in view of the above amendment.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

Claims 1-21 and 29-49 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. More specifically, Claims 1-21 and 29-49 stand rejected for insufficient antecedent basis for certain limitations recited in each of these claims. Applicants amend Claims 1-21 and 29-49 to correct the antecedent basis issues identified by the Examiner and therefore respectfully request the Examiner to reconsider and withdraw the rejection of Claims 1-21 and 29-49 under 35 U.S.C. §112, second paragraph.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The Office Action rejects Claims 1-49 as being anticipated by U.S. Patent No. 5,758,112 of Yeager, *et al.*, (hereinafter "Yeager"). Applicants respectfully traverse this rejection on the basis of the above amendments and the following arguments, and further contend that Yeager fails to disclose all elements of these amended claims, as described below, and hence, does not anticipate the claimed inventions.

For purposes of clarity in the discussion below, the respective claim rejections under 35 U.S.C. §102 are discussed separately.

A. Rejection of Claims 1-20 under 35 U.S.C. §102(b):

The Office Action rejects Claims 1-20 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the amendment to Claim 1 above and the following arguments, and further contend that Yeager fails to disclose all elements of these claims, as amended, and hence does not anticipate the claimed invention.

Claims 2-20 depend directly or indirectly upon amended Claim 1 and thereby incorporate the patentable features of amended Claim 1.

Amended Claim 1 is directed to a method performed in a microprocessor performing speculative instruction execution. The method includes a step of providing a structure to track register allocation for a first thread of the microprocessor. The method also includes a step of tracking a first set of pointers in the structure designed to manage the register allocation for an instruction of the first thread of the microprocessor to prevent a register allocated as a destination operand for the instruction from being overwritten before the instruction retires. The first set of pointers includes at least two pointers set apart by a fixed distance that move in unison up and down the structure.

An advantage of the method of the present invention is the ability to perform an instruction pipeline flush without having to physically restore register values.

The Yeager patent is directed to a method and apparatus for storing register renaming information in the event of a branch misprediction. Yeager discloses redundant mapping tables for use in microprocessors that rename registers and perform branch prediction. The redundant mapping tables include a number of primary RAM cells coupled to a number of redundant RAM cells. In the event of a branch instruction, the redundant RAM cells can save the contents of the primary RAM cells in a single clock cycle before the microprocessor decodes and executes subsequent instructions along a predicted branch path. Should the branch instruction be mispredicted, the redundant RAM cells can restore the primary RAM cells in a single clock cycle. To accomplish this, Yeager discloses a free register list coupled to a mapping table, which in turn is coupled to an instruction queue and the instruction queue is coupled to a register file. The free register lists disclosed by Yeager each include a read pointer and write pointer to identify entries in selected RAMs. Yeager moves the write pointer in increments determined by the member of instructions which graduate during each clock cycle. Likewise, Yeager moves the read pointer in increments by the number of free registers assigned during each clock cycle. The Yeager patent does not anticipate amended Claim 1.

The Yeager patent discloses two separate structures for tracking register allocation for instructions. Each such structure disclosed by Yeager includes two pointers, a read pointer and a

write pointer that operate independent of each other. In contrast, amended Claim 1 recites a step of tracking in a structure a set of pointers that includes at least two pointers set apart by a fixed distance and move in unison up and down the structure. The Yeager patent does not disclose two pointers set apart by a fixed distance that move in unison up and down a structure to track register allocation of a first thread of a microprocessor. In fact, the Yeager patent discloses that the read pointer of the free list is incremented by the number of free registers assigned during each cycle. While the write pointer is incremented by the number of instructions with graduate during each cycle. Hence, the read pointer and the write pointer in each structure disclosed by Yeager do not move in unison, but rather independently.

Yeager fails to anticipate amended Claim 1 and hence, fails to anticipate Claims 2-20, which depend directly or indirectly upon amended Claim 1. Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of Claims 1-20 under 35 U.S.C. §102(b).

B. Rejection of Claim 21 Under 35 U.S.C. §102(b):

The Office Action rejects Claim 21 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that Yeager fails to disclose all elements of this claim as described below, and hence, does not anticipate the claimed invention.

Claim 21 is directed to a method performed in a multithreading processor performing speculative instruction execution. Performance of the method provides a structure to track register allocation for a first thread and a second thread of the multithreading microprocessor. The method includes a step of tracking a first set of pointers in the structure assigned to manage register allocation of an instruction of the first thread of the multithreading processor and includes a step of tracking a second set of pointers in the structure assigned to manage the register allocation of an instruction of the second thread of the multithreading processor. Claim 21 is not anticipated by Yeager.

The Yeager patent discloses two independent free register lists for managing register allocation. Specifically, free register list (208) manages registers associated with floating point instructions and free register list (210) manages registers associated with integer related instructions. Nowhere does Yeager disclose that the floating point free register list and the integer free register list are a single structure. In contrast, Claim 21 recites a step of providing a structure to track register allocation for a first thread and a second thread of the multithreading processor. Performance of the method recited in Claim 21 tracks at least two sets of pointers in the provided structure. Nowhere does Yeager disclose the tracking of two sets of pointers in a structure. Yeager tracks one set of pointers in a first structure and a second set of pointers in a second structure. Accordingly, the microprocessor disclosed by the Yeager patent has an architecture, operation and function different from the architecture, function and operation of the method performed in a multithreading microprocessor performing speculative instruction execution recited in Claim 21.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 21 under 35 U.S.C. §102(b).

C. Rejection of Claims 22-27 Under 35 U.S.C. §102(b):

The Office Action rejects Claims 22-27 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the above amendments and the following arguments, and further contend that Yeager fails to disclose all elements of these claims as amended, and hence, does not anticipate the claimed invention.

Claims 21-27 depend, directly or indirectly upon amended Claim 22 and therefore incorporate the patentable features of amended Claim 22.

Amended Claim 22 is directed to a semiconductor device having a number of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out of order execution. The semiconductor device includes a first module providing a structure for holding information identifying available physical registers for the microprocessor and a first set of register pointers assigned to a first portion of the structure. The

first set of register pointers track the physical registers assigned as destination registers for a first thread of the microprocessor. The first set of register pointers includes a retire row pointer to identify where a pointer pointing to at least one of the physical registers assigned as a destination register for an instruction in the first thread that is next to be retired. The Yeager patent does not anticipate amended Claim 22 because Yeager fails to disclose a retire row printer.

Yeager discloses a read pointer and a write pointer, however, Yeager does not disclose a retire pointer. The Yeager patent discloses a graduation mask used to identify which instruction graduated. A mask is not a pointer. A mask is a binary value used to selectively screen out or let through certain bits and a value. In contrast, a pointer is a variable that contains the address of a storage location.

Amended Claim 22 is not anticipated by the Yeager reference. Amended Claim 22 recites a semiconductor device that includes a first set of register pointers and included in the set of register pointers is a retire row pointer to identify where a pointer is pointing to at least one of the physical registers assigned as a destination register for an instruction in a thread is next to be retired. Nowhere does Yeager disclose a retire row pointer. The Yeager patent is merely concerned with a read pointer and a write pointer and does not discuss a retire row pointer. Accordingly, the Yeager patent discloses a semiconductor device having a structure, operation and function, different from the structure, operation and function of the semiconductor device recited in amended Claim 22. Accordingly, Yeager does not anticipate amended Claim 22 or dependent Claims 23-27.

Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 22-27 under 35 U.S.C. §102(b).

D. Rejection of Claim 28 Under 35 U.S.C. §102(b):

The Office Action rejects Claim 28 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that Yeager fails to disclose all elements of this claim, as described below, and hence, does not anticipate the claimed invention.

Claim 28 is directed to a semiconductor device having a number of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out of order execution. The semiconductor device includes a first module providing a structure for holding information identifying available physical registers of the microprocessor, a first set of register pointers assigned to a first portion of the structure and a second set of registers assigned to a second portion of the structure. The Yeager patent does not anticipate Claim 28.

The Yeager patent discloses a first structure for holding information identifying available physical registers in a floating point instruction pipeline and a second structure for identifying available physical registers and a second pipeline or integer instruction pipeline of the microprocessor. In contrast, the semiconductor device of Claim 28 discloses a structure partitionable to hold at least two sets of register pointers to track the assignment of destination registers for at least two threads of a microprocessor performing out of order execution. Nowhere does the Yeager patent disclose a partitionable structure to track physical register assignments corresponding to either two threads or two instruction pipelines of a microprocessor. The Yeager patent discloses a single structure for each thread or instruction pipeline that includes a set of register pointers assigned to track physical registers assigned as destination registers for instructions in each respective thread or instruction pipeline. Accordingly, the semiconductor device of the Yeager patent has an architecture and a structure along with a function and an operation different from the architecture, structure, function, and operation of the semiconductor device of Claim 28. Hence, the Yeager patent does not anticipate Claim 28. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 28 under 35 U.S.C. §102(b).

E. Rejection of Claims 29-48 under 35 U.S.C. §102(b):

The Office Action rejects Claims 29-48 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the amendment to Claim 29 above and the following arguments, and further contend that Yeager fails to disclose all elements of these claims, as amended, and hence does not anticipate the claimed invention.

Claims 30-48 depend directly or indirectly upon amended Claim 29 and thereby incorporate the patentable features of amended Claim 29.

Amended Claim 29 is directed to a computer readable medium holding computer executable instructions for performing a method in a microprocessor performing speculative instruction execution. The method includes a step of providing a structure to track register allocation for a first thread of the microprocessor. The method also includes a step of tracking a first set of pointers in the structure designed to manage the register allocation for an instruction of the first thread of the microprocessor to prevent a register allocated as a destination operand for the instruction from being overwritten before the instruction retires. The first set of pointers includes a first pointer and a second pointer set apart by a fixed distance that move in unison up and down the structure.

The Yeager patent discloses two separate structures for tracking register allocation for instructions. Each such structure disclosed by Yeager includes two pointers, a read pointer and a write pointer that operate independent of each other. In contrast, amended Claim 29 recites a step of tracking in a structure a set of pointers that includes a first pointer and a second pointer set apart by a fixed distance and move in unison up and down the structure. The Yeager patent does not disclose two pointers set apart by a fixed distance that move in unison up and down a structure to track register allocation of a first thread of a microprocessor. In fact, the Yeager patent discloses that the read pointer of the free list is incremented by the number of free registers assigned during each cycle. While the write pointer is incremented by the number of instructions with graduate during each cycle. Hence, the read pointer and the write pointer in each structure disclosed by Yeager do not move in unison, but rather independently.

Yeager fails to anticipate amended Claim 29 and hence, fails to anticipate Claims 30-48, which depend directly or indirectly upon amended Claim 29. Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of Claims 29-48 under 35 U.S.C. §102(b).

F. Rejection of Claim 49 Under 35 U.S.C. §102(b):

The Office Action rejects Claim 49 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that Yeager fails to disclose all elements of this claim as described below, and hence, does not anticipate the claimed invention.

Claim 49 is directed to a computer readable medium holding computer executable instructions for performing a method in a multithreading processor performing speculative instruction execution. Performance of the method provides a structure to track register allocation for a first thread and a second thread of the multithreading microprocessor. The method includes a step of tracking a first set of pointers in the structure assigned to manage register allocation of an instruction of the first thread of the multithreading processor and includes a step of tracking a second set of pointers in the structure assigned to manage the register allocation of an instruction of the second thread of the multithreading processor. Claim 49 is not anticipated by Yeager.

The Yeager patent discloses two independent free register lists for managing register allocation. Specifically, free register list (208) manages registers associated with floating point instructions and free register list (210) manages registers associated with integer related instructions. Nowhere does Yeager disclose that the floating point free register list and the integer free register list are a single structure. In contrast, Claim 49 recites a step of providing a structure to track register allocation for a first thread and a second thread of the multithreading processor. Performance of the method recited in Claim 49 tracks at least two sets of pointers in the provided structure. Nowhere does Yeager disclose the tracking of two sets of pointers in a structure. Yeager tracks one set of pointers in a first structure and a second set of pointers in a second structure. Accordingly, the microprocessor disclosed by the Yeager patent has an architecture, operation and function different from the architecture, function and operation of the method performed in a multithreading microprocessor performing speculative instruction execution recited in Claim 49.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 49 under 35 U.S.C. §102(b).

CONCLUSION

In view of the remarks set forth above, Applicants believe that the present invention is in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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Respectfully submitted,

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